



K.S.R.M. COLLEGE OF ENGINEERING (UGC-AUTONOMOUS)

Kadapa, Andhra Pradesh, India- 516 003

Approved by AICTE, New Delhi & Affiliated to JNTUA, Ananthapuramu.

An ISO 14001:2004 & 9001: 2015 Certified Institution



Lr./KSRMCE/ (Department of E.C.E)/2021-22/

Date: **07.02.2022**

To

The Principal,
K.S.R.M.College of Engineering
Kadapa.

Respected Sir,

Sub: KSRMCE - (Department of E.C.E) - Subject - Requested - Reg. **conducting a Guest lecture for students.**

It is being brought to your kind notice that, With reference to the cited, the department of Electronics & Communication engineering would like to conduct a Guest lecture on "**RTL Design and Verification using VLSI**" in association with ECHO on **09-02-2022**. The objective of this workshop is to introduce basic and recent developments in the field of VLSI. As the coordinator, I would like to request your support and permission to conduct this event in virtual mode (Google Meet) from 11:00 AM to 12:00 PM. The participants will be third year students of ECE and faculty.

Thanking you

Yours Faithfully

Dr. Syed Zahiruddin
Associate Professor
Coordinator

Cc:

To All Deans /HoD's

*Forwarded to the
principal sir
G. H.*

*Permitted
V. S. S. Mm/5
07/02/2022*



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No./Circular/1.

Date: 08-02-2022

CIRCULAR

It is hereby informed that A Guest Lecture on “RTL Design and Verification using VLSI” is going to be organized by department of ECE on 09-02-2022, from 11:00 AM to 12:00 PM through virtual mode (Google Meet).

Google meet link is

<https://zoom.us/j/96546068651?pwd=YzVGTY9GLzMyU2d0L09QanBjcEorZz09>

In this connection, all the third year ECE students and faculty are hereby directed to attend the lecture without fail.

V. S. S. Murthy

Principal
PRINCIPAL

K.S.R.M. COLLEGE OF ENGINEERING
KADAPA - 516 003. (A.P.)



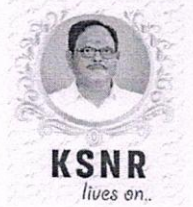
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Department of Electronics and Communication Engineering

**A Guest Lecture
On**

"RTL Design and Verification using VLSI"

09th February, 2022

REPORT

Target Group : Faculty & Students

Details of Participants : 05 Faculty and 78 Students

Coordinator : Dr. S. Zahiruddin, Associate Professor, ECE Dept.,

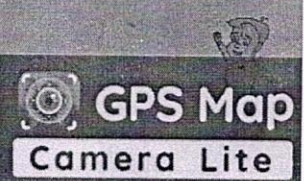
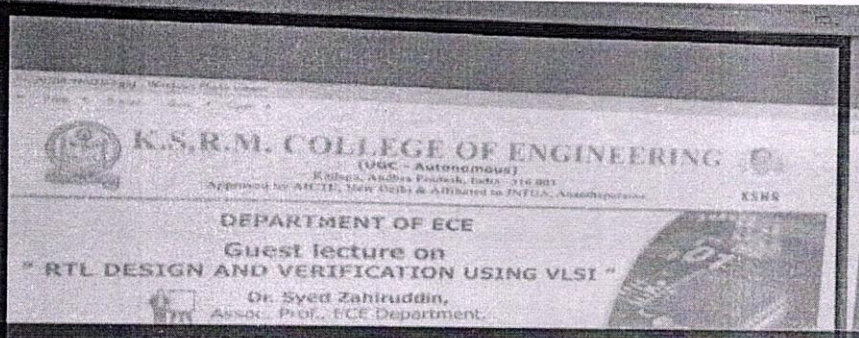
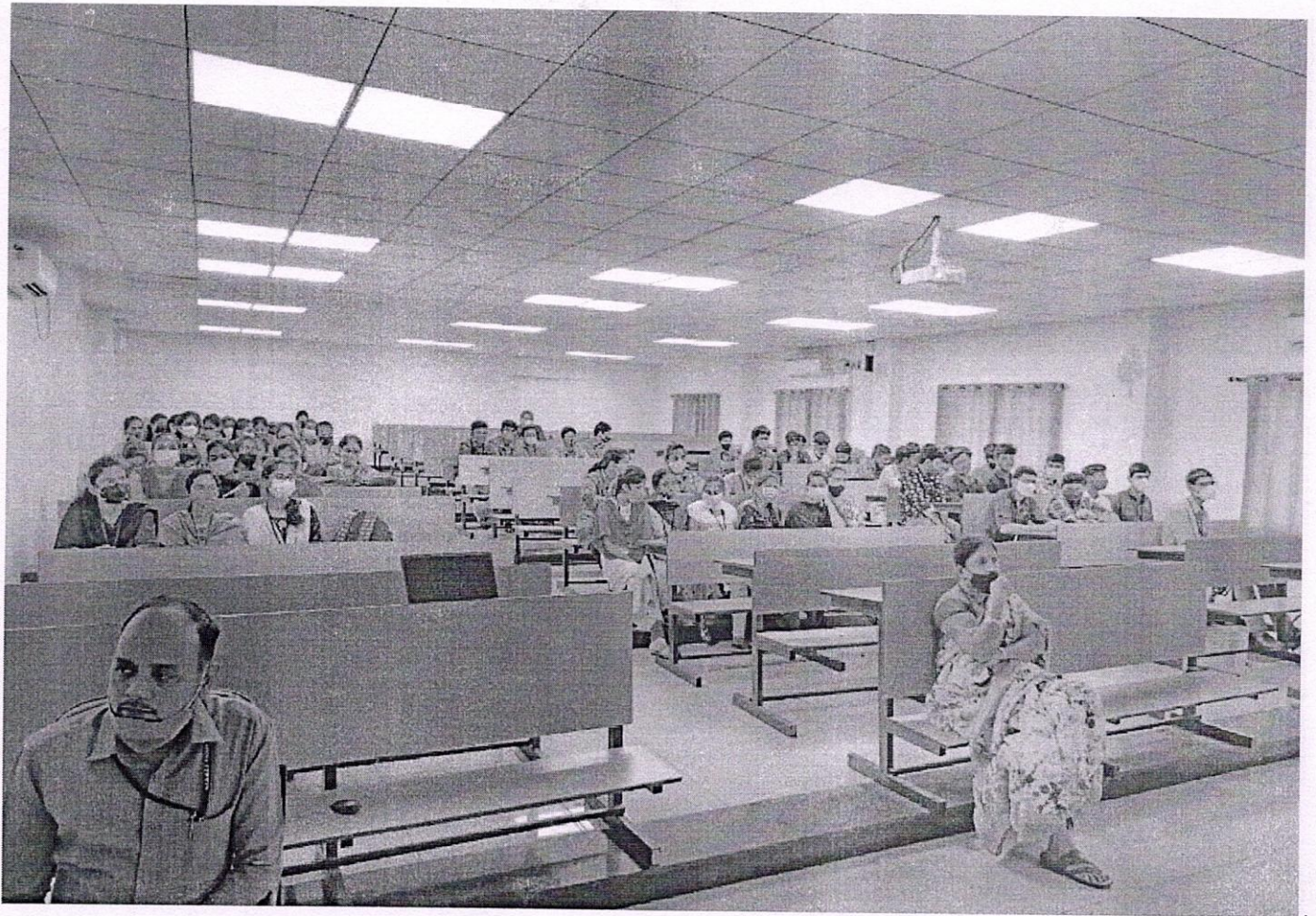
Co-coordinator : Sri. M. Prabhakar, Assistant Professor, ECE Dept.,

Organizing Department: Electronics & Communication Engineering

Venue : SJ Seminar Hall, Virtual Mode (Google Meet)

Resource person : Sri. M. Madana Gopal, Corporate Trainer & Placement Consultant, AARK IC Technologies Pvt. Ltd., Bangalore, Karnataka-560038.

Register Transfer Level (RTL) is an abstraction for defining the digital portions of a design. It is the principle abstraction used for defining electronic systems today and often serves as the golden model in the design and verification flow. The RTL design is usually captured using a hardware description language (HDL) such as Verilog or VHDL. While these languages are capable of defining systems at other levels of abstraction, it is generally the RTL semantics of these languages, and indeed a subset of these languages defined as the synthesizable subset. This means the language constructs that can be reliably fed into a logic synthesis tool which in turn creates the gate-level abstraction of the design that is used for all downstream implementation operations. RTL is based on synchronous logic and contains three primary pieces namely, registers which hold state information, combinatorial logic which defines the next state inputs and clocks that control when the state changes.



Tadigotla Village, Chintakommadinne Mandal, Pulivendula Road
KSRM Hostel Road Andhra Pradesh 516003, Andhra Pradesh
516003, India

Latitude
14.4767332°

Longitude
78.765078°

Local 11:01:30 AM
GMT 05:31:30 AM

Altitude 54.5 meters
Wednesday, 09-02-2022

Co-ordinators:

- 1. Dr. Syed Zahiruddin
- 2. Sri. M. Prabhakar

V. S. S. Murthy
Principal
PRINCIPAL
K.S.R.M. COLLEGE OF ENGINEERING
KADAPA - 516 003. (A.P.)

List of the participants:

S. No.	Name of the student	Roll No.
1.	G. Anusha	199Y1A0441
2.	G.K.S. Sree Dhanya	199Y1A0451
3.	D. Mounika	199Y1A0432
4.	K. Anusha	199Y1A0457
5.	J. Anjali	199Y1A0455
6.	A. Lavanya	199Y1A0404
7.	G. Navya	199Y1A0442
8.	C. Sai Susmitha	199Y1A0421
9.	K. Sree Vidya	199Y1A0463
10.	G. Swarnalatha	199Y1A0444
11.	K. Kaveetha	199Y1A0447
12.	C. Neetha	199Y1A0429
13.	D. Varshini	199Y1A0434
14.	A. Mounika	199Y1A0405
15.	B. Sangeetha	199Y1A0410
16.	C. Geetha Priya	199Y1A0426
17.	K. Sravani	199Y1A0465
18.	K. Kajabee	199Y1A0462
19.	D. Anusha	199Y1A0435
20.	K. S. Gowthami	199Y1A0458
21.	K. Sumithra	199Y1A0474
22.	K. Archana	199Y1A0477

23.	M. Harika	199Y1A0492
24.	K. Eeshitha Rachana	199Y1A0473
25.	M. Sreevani	199Y1A0489
26.	P. Lingeswari	199Y1A04C0
27.	P. Naveena	199Y1A04C6
28.	N. Maneesha	199Y1A04B1
29.	R. Keerthana	199Y1A04C8
30.	S. Lakshmi Prasanna	199Y1A04D1
31.	S. Sujita	199Y1A04D4
32.	R. Niharika	199Y1A04C7
33.	M. Sudharani	199Y1A0493
34.	G. Vijay	209Y5A0405
35.	K. Aravind Kumar	209Y5A0409
36.	S. Sudarshan	199Y1A04F0
37.	V. Yuvaraju	199Y1A04H4
38.	K. Mohan Vamsi	209Y5A0408
39.	S. Jafrullah	199Y1A04D8
40.	S. Jeelan	199Y1A04E0
41.	S. M. D. Ghouse	199Y1A04E3
42.	V. Venkata Ramana Reddy	199Y1A04H5
43.	S. Bala Siddartha	209Y5A0418
44.	K. Manoj Kumar	199Y1A0464
45.	G. Upendra	199Y1A0440
46.	K. Sai Bharath	199Y1A0441

47.	D. Vikas	199Y1A0437
48.	J. Vinod	199Y1A0456
49.	C. Veera siva	199Y1A0430
50.	K. Janardhan	199Y1A0467
51.	K. Chandra sekhar reddy	199Y1A0476
52.	G. Shaif	199Y1A0454
53.	G. Prasanna Kumar	199Y1A0448
54.	G. Sharath	199Y1A0452
55.	G. Sai Sumanth	199Y1A0453
56.	K. Sagar	199Y1A0460
57.	C. Varaprasad reddy	199Y1A0422
58.	A. Venkata pavan kumar reddy	199Y1A0407
59.	A. Venkatesh	199Y1A0401
60.	C. Sai Dheeraj	199Y1A0427
61.	B. Ajay Kumar	199Y1A0408
62.	C. Tejesh kumar reddy	199Y1A0418
63.	B. V. Sainath reddy	199Y1A0415
64.	B. V. Tarun kumar	199Y1A0413
65.	B. Sreenath	199Y1A0412
66.	C. Sandeep Reddy	199Y1A0428
67.	G. Madhavan	199Y1A0445
68.	N. Brahmam	199Y1A04A8
69.	E. Neelavathi	209Y5A0402
70.	G. Nishmaja Pravallika	209Y5A0406

71.	L. Niharika	209Y5A0410
72.	P. Venkata Lakshmi	209Y5A0416
73.	T. Manasa	209Y5A0419
74.	M. Venkata Harika	209Y5A0413
75.	V. Swetha	199Y1A04G9
76.	P. Bhumika	199Y1A04B3
77.	M. Sravanthi	199Y1A04A6
78.	N. Poornima	199Y1A04A9

Photos of the event:



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KSNR
lives on.

DEPARTMENT OF ECE

**Guest lecture on
" RTL DESIGN AND VERIFICATION USING VLSI "**



Dr. Syed Zahiruddin,
Assoc. Prof., ECE Department.



09-02-2022,
11 AM to 12 PM.



SJ - Seminar Hall
(Online mode)

Coordinator

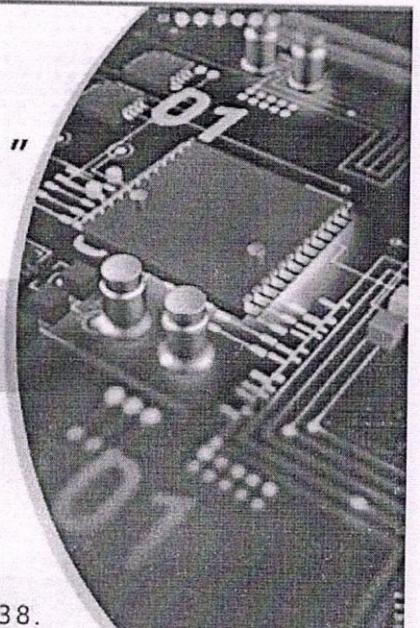
Dr. Syed Zahiruddin,
Assoc. Prof., ECE Department.

CO-Coordinator

Sri. M. Prabhakar,
Asst. Prof., ECE Department.

Resource person :

Sri. M. Madan Gopal,
Corporate Trainer & Placement Consultant,
AARK IC Technologies Pvt Ltd, Bangalore, Karnataka 560038.



Dr. G. Hemalatha
(VCO)

Dr. V.S.S. Murthy
(Principal)

Dr. Kandula Chandra Obul Reddy
(Managing Director)

Smt. K. Rajeswari
(Correspondent Secretary, Treasurer)

Sri K. Madan Mohan Reddy
(Vice - Chairman)

Sri K. Raja Mohan Reddy
(Chairman)

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